When Stability Meets Noise: Investigating Load-Dependent Timing Accuracy and Jitter in 555 Timer Oscillators

Omar Mubarak

Abstract

The performance of a 555 timer astable oscillator is often assessed through power-rail voltage fluctuations, but it's unclear whether fluctuations' magnitude alone predicts timing instability. This study investigates that question by comparing three circuit configurations—a version with an unmodified design, a version with decoupling capacitors, and a version adding a transistor switching stage—across three electrical loads (100 Ω, 1,000 Ω, and 10,000 Ω) and eight resistor configurations. Because standard laboratory equipment was not available, a custom ESP32-based measurement system was developed and calibrated to characterize voltage (±0.01 V accuracy) and period, using MCPWM capture and NTP-based clock calibration, which produced an estimated clock frequency of 80.0006907 MHz. Results show that RMS power-rail noise varied only modestly (approximately 0.02–0.12 V) while period jitter varied by more than two orders of magnitude (roughly 3.58 µs to over 370 µs), indicating that operating frequency and circuit configuration have substantially greater influence on timing stability than power-rail voltage fluctuations alone. No single configuration was superior: Version 1 achieved the lowest mean frequency error, Version 2 decreased frequency variability under several conditions, and Version 3 performed best under heavy loading and reduced peak-to-peak voltage transients effectively. These findings suggest that timing jitter in the 555 timer is influenced by a complex interaction between operating frequency, electrical loading, circuit architecture, and power-rail disturbances rather than voltage fluctuations' magnitude alone.

1. Introduction

Pulse trains are among the most versatile electrical waveforms and have numerous applications in signal processing, digital audio and communication systems due to their simple structure. As the information they convey is dependent on the timing of rising and falling edges, it is important that each successive cycle has the same duration. However, in practice, fluctuations during the operation of pulse train generators cause random deviations in each cycle's duration, a phenomenon commonly known as jitter. This is particularly prominent in relaxation oscillators, where timing is susceptible to changes based on different factors in the circuit's environment, as shown in the study by Abidi and Meyer (1983), where multiple factors like the slope of capacitor charging and low-frequency noise affect the pulse train generator's stability.

The 555 timer was chosen for its popularity and flexibility. In astable mode, the circuit operates as a relaxation oscillator, where a timing capacitor charges and discharges between certain thresholds, which determines the pulse train's period. With each capacitor cycle, fluctuations in the circuit's state variables cause jitter. Since the timing capacitor's rate of charging is affected by voltage at the power rails, power rail RMS noise, a common representation of the magnitude of power rail voltage fluctuations, is expected to be associated with timing accuracy in a relaxation oscillator. Therefore, the 555 timer provides an opportunity to investigate the extent to which voltage fluctuations affect timing accuracy in relaxation oscillators.

This study investigates that problem using a 555 timer operated in astable mode. Rather than treating circuit modification as a search for a single universally superior configuration, the investigation compares three circuit versions under different electrical loads and timing conditions. Version 1 represents the original circuit, version 2 introduces a 10 nF capacitor on the control voltage pin together with 100 nF and 10 µF power rail capacitors, and version 3 retains those modifications while adding a 2N2222A transistor switching stage. Eight measured resistor combinations were tested with 100 Ω, 1 kΩ, and 10 kΩ loads, producing 24 test conditions for each circuit version. This experimental design allows the relationships between circuit modification, electrical loading and timing behaviour to be evaluated across a range of operating frequencies rather than under a single nominal condition.

A second component of the investigation is the measurement methodology. Because conventional laboratory equipment was unavailable, an ESP32 development board was adapted into a measurement system for voltage and period. The voltage measurement system was calibrated against known voltages, while several approaches to period measurement were investigated before MCPWM capture was selected. The ESP32 clock

was subsequently calibrated. The resulting instrumentation was used to characterize relative frequency error, absolute timing jitter, RMS power rail noise, and peak-to-peak voltage excursions, allowing electrical disturbances and timing behaviour to be evaluated together.

The purpose of this study is therefore not to identify one circuit version as universally best, but to determine how operating frequency, electrical loading, circuit configuration, and the representation of power rail disturbance interact to influence timing accuracy and stability. This distinction is important because the experimental results indicate different performance tradeoffs among the three configurations. By combining controlled circuit modifications with calibrated low-cost embedded instrumentation, this investigation seeks to provide a more complete characterization of the practical behaviour and limitations of the 555 timer as a pulse-train generator.

1.1. Literature Review

The relationship between power rail RMS noise and jitter is not necessarily direct. The timing variation in a single pulse depends on the circuit's sensitivity to power rail RMS noise rather than power rail RMS noise alone. Herzel and Razavi (1999) developed relationships between supply and substrate noise and oscillator jitter in terms of the sensitivity of oscillation frequency to those disturbances. More generally, the characteristics of the disturbance can influence timing behaviour in ways that are not captured by a single amplitude measurement. Shi et al. (2018) showed, for example, that the jitter of a ring oscillator under sinusoidal supply interference depends on both the amplitude and frequency of the interfering signal. These results suggest that a scalar measure such as RMS voltage noise may not, by itself, fully characterize the timing consequences of a disturbance.

The sensitivity of an oscillator to supply disturbances is also an important design consideration. Arakali et al. (2010) demonstrated that supply noise can significantly affect oscillator-based timing systems and developed analytical relationships describing supply noise sensitivity. Their results reinforce the distinction between the presence of electrical noise and the extent to which that noise is converted into timing uncertainty. Consequently, circuit modifications intended to suppress supply disturbances cannot automatically be expected to improve every aspect of oscillator performance. A reduction in voltage fluctuations may coexist with substantial timing variability, while a modification associated with improved timing stability under one loading condition may not provide the smallest frequency error under another.

2. Methods

2.1. Measurement Instrumentation

Before gathering data, there was an important subject to be addressed: measurement. Standard laboratory equipment like function generators and oscilloscopes were not available. Thus, a measurement system built using either the ESP32 development board or the Arduino Uno R3 was required.

Building on the characteristics of both boards, the ESP32 development board was found to be more suitable, as it featured an ADC resolution that is four times that of the Arduino's and a clock frequency that is five times as fast as the Arduino's. The development of the ESP32 as a measurement tool went through seven versions: four for voltage measurement and three for period measurement.

All resistors and capacitor values were measured using a multimeter, so that component tolerances do not introduce significant errors.

Voltage Measurement

Version 1. The ESP32's ADC was known for its non-linearity, so calibration needed to be done first. For this, the ESP-IDF framework offers an ADC calibration library. Using this calibration library, the ESP32 displayed significantly corrected voltage output. By using samples with a size of 100, the measurement reflected the actual voltage. With a 1.28 MΩ-99.3 kΩ voltage divider, the ESP32's accuracy further improved. Attenuation of the input was unnecessary, since at 0 dB attenuation, the ADC has the best accuracy. Though, with this design, there was an issue. The high impedance of the voltage divider caused ADC measurements to slowly drift then be corrected again. The ADC required an impedance less than 100 kΩ, and the impedance of the voltage divider was an order of magnitude greater.

Version 2. After reducing the input impedance (6.1 kΩ-986 Ω), and monitoring the output of a buffer-amplified voltage divider test circuit, the ADC drift was now diminished, but error was still present even with using samples. Hence, the ADC needed manual calibration.

Version 3. By collecting 81 samples of ESP32 measurements and actual measurements through a multimeter, the difference between ESP32 and actual measurements was found, and as a function of the actual voltage values, the difference did not vary linearly; rather, the difference was approximately constant across all measurements. Hence, the calibration constant was identified as -17 mV.

Version 4. The voltage readings were rounded to two decimal digits instead of truncating, which further improved accuracy and decreased randomness that was present in the third decimal digit.

With the modifications, the ESP32 was able to measure input voltages with ±0.01 V error at most, providing a limited but reliable way to observe voltages at the power rails.

Period Measurement

Version 1. The ESP32 offers many methods for measuring periods, which were implemented in the following progression: (1) a timer-interrupt system then (2) the RMT peripheral then (3) the MCPWM capture peripheral. First, a timer-interrupt system was considered. Timers are assigned interrupts, such that, at an edge, the interrupt is called, the timestamp of the interrupt is captured, and the period is, based on the difference of edge timestamps, computed, but with a caveat: edge timestamps are ahead of timer-called interrupts, since calling an interrupt has delay. Therefore, using timers for period measurement might introduce error. Next, to mitigate interrupt delay, the a system based on the RMT peripheral was implemented. The RMT peripheral captures timestamps independently of interrupts. However, it has limited storage memory, and it is meant for capturing entire signals rather than edge timestamps. Hence, the RMT peripheral was also incompatible for this use case. The selected option was the MCPWM capture peripheral, which has a similar mechanism to the timer-interrupt system with the only difference being that an edge's timestamp is captured independently of interrupt calls. Therefore, it guaranteed that timestamps are reported without modification.

Testing the ESP32 against a pulse generator implemented through an Arduino Uno R3, a significant deviation of up to 1304 ppm from the expected period was present in the measurements, and the error was relatively constant with respect to frequency. This suggested that the error was in either or both clocks (the ESP32's and the Arduino's).

Version 2. Shifting focus to the circuit, a transistor was used for switching. However, since the input HIGH voltage is greater than the ESP32's power rail voltage, transistor switching was delayed slightly because of deep saturation. Using a voltage divider rather than an MPS12A transistor for switching decreased switching delay by 5 µs when tested on the Arduino's function generator.

Version 3. Because of the 1300+ ppm error, either clock needed to be calibrated to calibrate the other. Since the ESP32 includes a WiFi module, it can be calibrated through NTP synchronization. The ESP32 connected to an NTP server then synchornized its clock with that of the NTP server then waited for 24-hours before polling the NTP server's clock time. Finally, the two times were compared, and the error was determined in ppm as in equation 2.1. After four trials, an average PPM error of -8.63375 was obtained. Using this error to calculate frequency as in equation 2.2 yielded 80.0006907 MHz, a value that

should only be taken as an estimate that is subject to uncertainty arising from NTP synchronization and network latency, rather than an exact measurement. However, this estimate is intented to better account for the rate error of the MCPWM capture module's clock.

$$E = \frac{T_{ESP} - T_{NTP}}{T_{NTP}} \times 10^6 \qquad \text{(Equation 2.1)}$$

$$F_{est} = \frac{F_{nominal}}{1 + E \times 10^{-6}} \qquad \text{(Equation 2.2)}$$

Hence, the measurement system was completed with the circuit shown in Figure 2.1 and the code posted on a GitHub repository (ZXSQ1 2026).

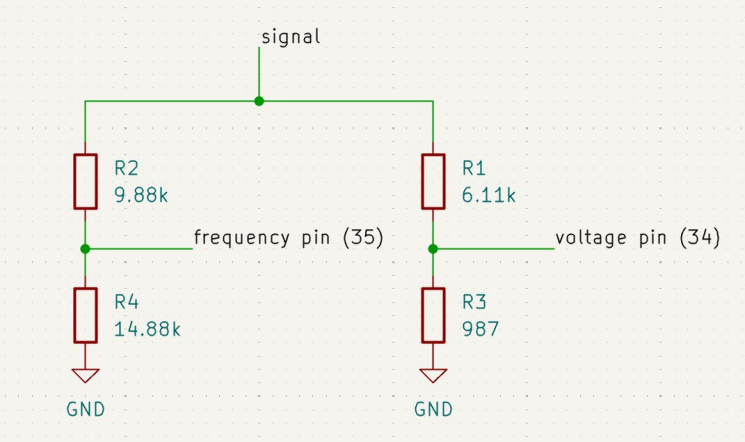


Figure 2.1. Final ESP32 measurement circuit.

2.2. Measurement Methodology

For each of the boards (the astable 555 timer circuit and the Arduino), performance was obtained across three versions, with each version adding features to its predecessor. For each version, collection was done through a script that extracts data from the ESP32 logs into CSV files.

Later analysis was performed using the Python programming language. Timing jitter was quantified as the population standard deviation of absolute period measurements as in equation 2.3. Frequency was quantified as the reciprocal of period measurements, and its relative error was expressed in parts per million (ppm) with respect to the expected frequency as in equation 2.4, where expected frequency depends on the circuit. For the 555 timer astable circuit, it is the frequency calculated through the equation in the datasheet (Texas Instruments 2023). For the Arduino Uno pulse generator, it is the frequency calculated through Timer1 variables (ZXSQ1 2026).

$$\sigma_T = \sqrt{\frac{\sum_{i=1}^{n} (T_i - \bar{T})}{n}} \qquad \text{(Equation 2.3)}$$

$$E_f = \left| \frac{f_m - f_0}{f_0} \right| \qquad \text{(Equation 2.4)}$$

Figure 2.2 shows the configuration for power rail noise measurement, while Figure 2.3 shows a similar configuration for period measurement.

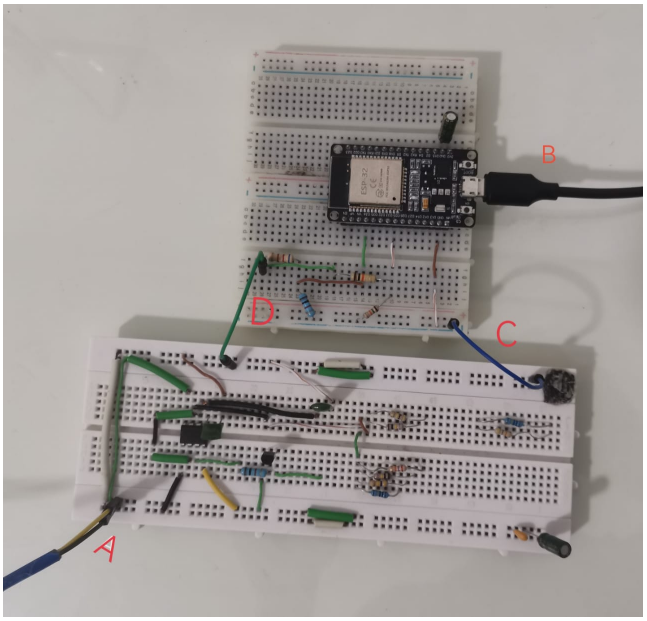


Figure 2.2. Power-rail noise measurement setup. **A:** *5V adapter power lines.* **B:** *ESP32 USB connected to laptop for serial communication.* **C:** *GND power line.* **D:** *Monitored VCC power line.*

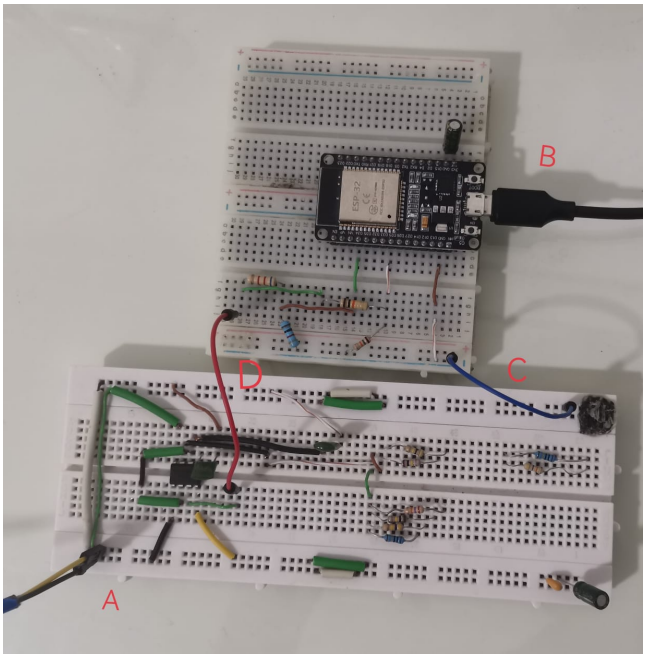


Figure 2.3. Period measurement setup. **A:** *5V adapter power lines.* **B:** *ESP32 USB connected to laptop for serial communication.* **C:** *GND power line.* **D:** *Monitored 555 output waveform.*

Arduino Uno R3 Test Procedures. In version 1, measurement was done with the basic pulse generator code without calibration or correction of clock errors. This is the stage in which the 1300+ ppm was observed. In version 2, the clock error was corrected. In version 3, 100 nF tantalum and 10 µF electrolytic capacitors were added at the power rails.

Each version was tested on eight frequencies: 1Hz, 5Hz, 10Hz, 50Hz, 100Hz, 200Hz, 500Hz, 1000Hz. However, they differed slightly from version to version, since corrections to clock frequency often lead to more quantization error. With supply rail noise measurement, each frequency was tested with three loads: 100 Ω, 1 kΩ, 10 kΩ. Loads were not considered in period measurement, since they did not have an apparent effect on switching.

A sample of size n = 20000 was collected for each frequency-load pair during the power rail noise measurement stage, and a sample of size n = 2000 was collected for each frequency setting during the period measurement stage. This is done for each of the three versions.

555 Timer Astable Mode Circuit Test Procedures. In version 1, the original circuit was used (Figure 2.4). In version 2, a 10 nF film capacitor was added to pin 5 (as advised by the datasheet) as well as 100 nF tantalum and 10 µF electrolytic capacitors at the power rails. In version 3, a 2N2222A transistor switching stage was added, where the timer's output was connected to base by a 1 kΩ resistor, VCC was connected to collector, and the circuit output was connected to emitter.

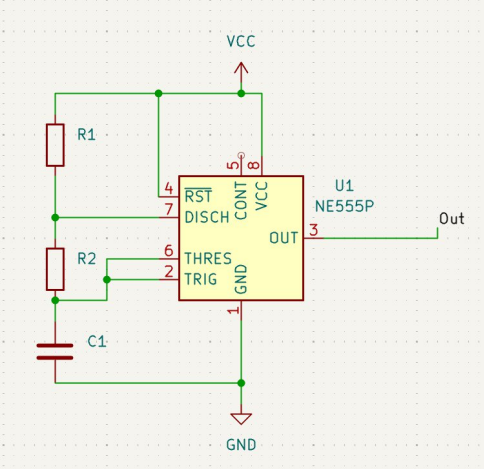


Figure 2.4. The unmodified, original 555 astable circuit.

The timing capacitor was a 10nF film capacitor. To test the circuit under multiple frequencies, eight resistor configurations were alternated (R1-R2): 100k-27k, 100k-100k, 100k-470k, 100k-1M, 470k-27k, 470k-100k, 470k-470k, 470k-1M. This was possible by using jumpers to manually switch between resistors in each configuration. Figures 2.2 and 2.3 show the two sets of resistors, where R1 is the upper set, and R2 is the lower set.

Additionally, for each resistance configuration, three loads where tested: 100 Ω, 1 kΩ, 10 kΩ.

This setup was used for both power rail noise measurement and period measurement, since, in a 555 astable mode circuit, the timing capacitors get charged from the power supply, which is affected by loads. Hence, jitter was expected to be influenced by loads.

For each frequency-load pair, a sample of size n = 20000 was collected in the power rail noise measurement stage, and a sample of size n = 2000 was collected in the period measurement stage. This is done for each of the three versions.

3. Results

3.1. Frequency Accuracy Across Circuit Configurations

Across all electrical loads (100 Ω, 1,000 Ω, and 10,000 Ω), version 1 achieved the lowest relative mean error—ranging from 32,351 ppm to 36,219 ppm—but exhibited severe variability under a heavy 100 Ω load with a standard deviation of 35,653 ppm (compared to 12,570 ppm at 10,000 Ω) as shown by the error bar in Figure 3.1.

Adding decoupling capacitors in version 2 increased mean error at higher load resistances (reaching 40,015 ppm at 1,000 Ω and 43,560 ppm at 10,000 Ω), but reduced error variability at 100 Ω down to a standard deviation of 29,343 ppm, stabilizing further to 10,305 ppm at 10,000 Ω.

The addition of transistor switching in version 3 resulted in the highest overall mean error at higher loads (44,304 ppm at 1,000 Ω and 45,181 ppm at 10,000 Ω). However, under a heavy 100 Ω load, version 3 not only achieved the lowest mean error across all tests at 27,795 ppm, but also dramatically stabilized variation, cutting the standard deviation to a low 12,996 ppm.

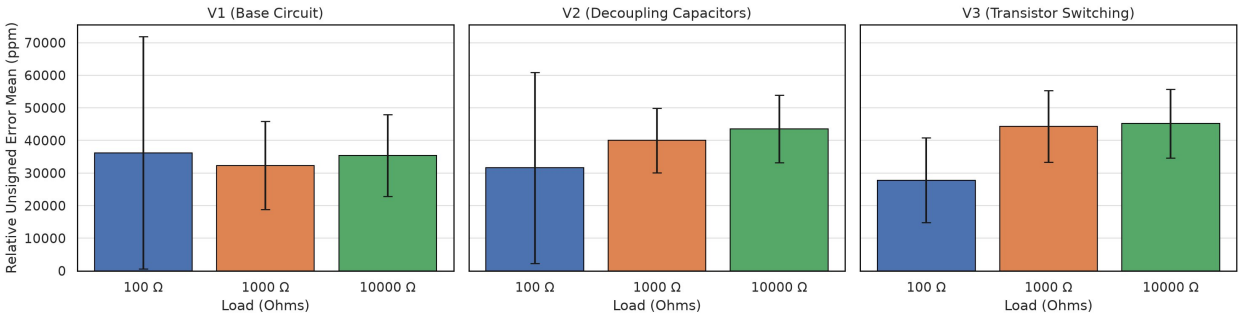


Figure 3.1. Frequency relative error across versions and loads.

3.2. Frequency- and Load-Dependent Timing Jitter

Timing jitter (1σ period, µs) was evaluated across different frequencies (from 55.98 Hz to 904.84 Hz) and electrical loads (100 Ω, 1,000 Ω, 10,000 Ω).

Timing jitter exhibited a strong inverse relationship with frequency across all configurations. At low frequencies (55.98 Hz), jitter peaked severely (reaching 370.63 µs in version 1 under a 100 Ω load). At higher frequencies (904.84 Hz), jitter dropped below 12 µs across all versions and loads.

Decoupling capacitors (version 2) consistently reduced timing jitter under heavy load conditions (100 Ω) at lower frequencies, cutting jitter at 55.98 Hz from 370.63 µs (version 1) down to 183.76 µs (version 2).

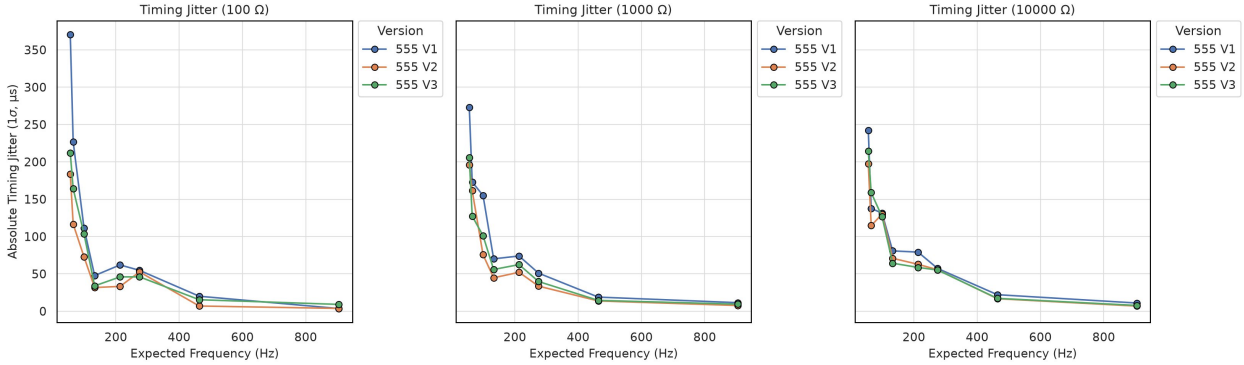


Figure 3.2. Timing jitter by frequency across circuit versions.

Pearson correlation coefficients between period and timing jitter were calculated for each version-load pair, with each coefficient calculated from eight period-jitter pairs representing the eight frequencies. Table 3.1 indicates strong, positive correlation between the two variables for all version-load pairs ($n = 8$, $p < 0.05$, $r > 0.94$).

Version	Load (Ω)	n	P-value	r
1	100	8	0.00041	0.94466
2	100	8	0.00039	0.94538
3	100	8	0.00007	0.96946
1	1,000	8	0.00008	0.96738
2	1,000	8	0.00003	0.97581
3	1,000	8	0.00010	0.96532
1	10,000	8	0.00029	0.95045
2	10,000	8	0.00051	0.94011
3	10,000	8	0.00001	0.98256

Table 3.1. Correlation coefficients for period-jitter relationships across versions and loads.

3.3. Power Rail Noise Dynamics Across Loads

Power rail noise was analysed through RMS voltage noise (V) and peak-to-peak voltage noise (V) across loads.

Baseline RMS noise remained low overall (<0.12 V), peaking at 100 Ω for version 1 (0.104 V) and version 3 (0.119 V) before dropping below 0.05 V at higher loads.

Peak-to-peak transient noise was suppressed drastically by circuit modifications. Version 1 exhibited severe peak-to-peak voltage swings between 2.72 V and 3.32 V. Adding decoupling capacitors (version 2) reduced these spikes to 1.26 V – 1.69 V, while transistor switching (version 3) achieved the greatest suppression (0.88 V – 1.09 V).

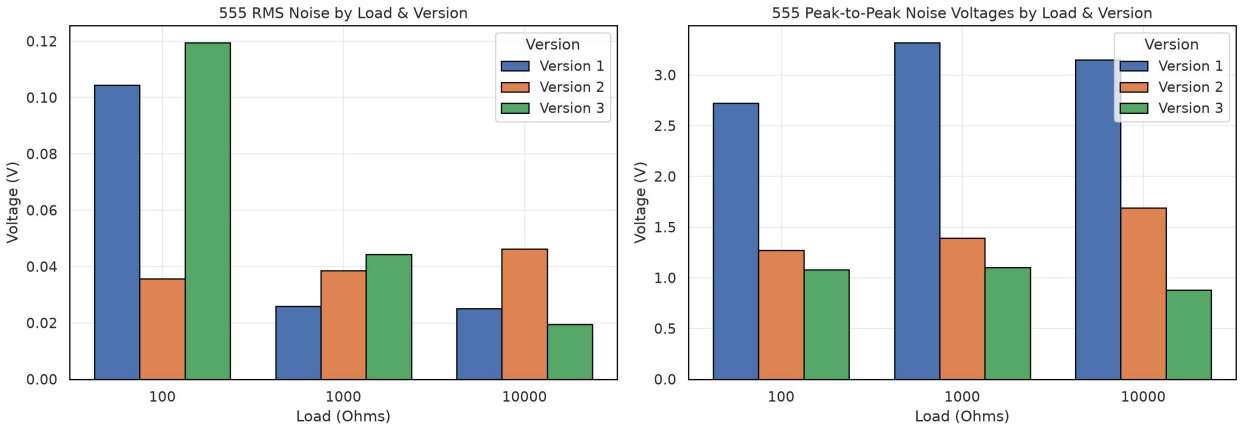


Figure 3.3. RMS noise & peak-to-peak noise voltages by load and version.

3.4. Relationship Between RMS Noise and Timing Jitter

A direct comparison of RMS power rail noise and timing jitter did not show a clear linear relationship. RMS noise remained within a relatively narrow range of approximately 0.02–0.12 V, while timing jitter varied by more than two orders of magnitude, from approximately 3.58 µs to greater than 300 µs.

The large variation in jitter despite the relatively small variation in RMS noise suggests that RMS power rail noise alone is insufficient to explain the observed timing instability. In particular, the strong dependence of jitter on operating frequency indicates that frequency and circuit configuration are likely more important factors within the tested conditions.

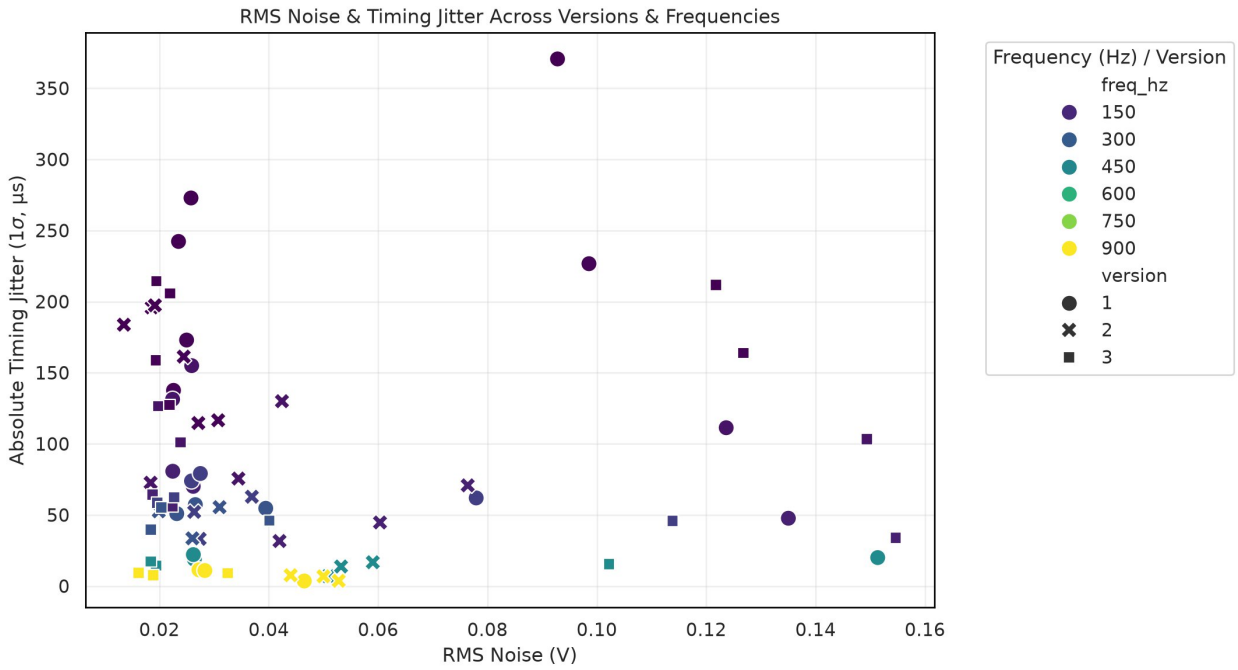


Figure 3.4. RMS noise & timing jitter across frequencies and versions.

Pearson correlation coefficients between power rail RMS noise and timing jitter were calculated for each version-load pair, with each coefficient calculated from eight noise-jitter pairs representing the eight frequencies. Table 3.2 indicates statistically insignificant correlation between RMS noise and timing jitter in most cases ($p > 0.05$) with the only exception of Version 2 at a load of 100Ω.

Version	Load (Ω)	n	P-value	r
1	100	8	0.92790	0.03849
2	100	8	0.03555	-0.74070
3	100	8	0.30045	0.41981
1	1,000	8	0.71705	-0.15329
2	1,000	8	0.07536	-0.65924
3	1,000	8	0.12250	0.59147
1	10,000	8	0.07606	-0.65807
2	10,000	8	0.12678	-0.58612
3	10,000	8	0.42646	0.32882

Table 3.2. Correlation coefficients for RMS noise-jitter relationships across versions and loads.

4. Discussion

The investigation examines the relationship between timing jitter and power rail RMS noise in 555 timer astable circuit performance with different loads and circuit versions. Specifically, it evaluates whether RMS noise alone adequately predicts timing jitter and investigates how circuit modifications and operating frequency relate to timing accuracy and stability. The results show that timing jitter and RMS noise were not significantly correlated. Rather, they show that timing jitter is more strongly correlated to other factors. This is significant, since the investigation does not aim to determine the 555 timer circuit version with the best performance. Instead, it outlines how certain modifications to the circuit lead to changes in some metrics.

Measuring frequency accuracy across different loads (100 Ω, 1,000 Ω, and 10,000 Ω) in Figure 3.1, no version exhibited superiority under all conditions. Version 1 had the least mean frequency error—ranging from 32,351 ppm to 36,219 ppm—but had the highest variability—a standard deviation of 35,653 ppm—under a heavy load of 100 Ω. In version 2, the range of mean frequency errors increased, and the variability under 100 Ω only decreased slightly. Version 3 achieved a variability close to a third of version 1's variability—a standard deviation of 12,996 ppm—although the range of mean frequency errors increased. This is present in version 3 only, which suggests that the transistor switching stage was responsible ($p < 0.05$, $r = 0.802$), as it reduced the direct loading on the 555 timer output pin (Sedra et al. 2020). Collectively, this suggests that no version was superior under all loads and that frequency mean error alone is not sufficient to describe frequency accuracy without considering jitter.

In Figure 3.2, jitter was measured against operating frequencies (from 55.98 Hz to 904.84 Hz) across different loads (100 Ω, 1,000 Ω, and 10,000 Ω). Across all versions, jitter seemed to increase at lower frequencies and decrease at higher frequencies ($p < 0.05$, $0.94 < r < 0.983$ across all versions and loads), which can be explained by the mechanism of relaxation oscillators (Texas Instruments 2023). With more time for capacitor charging and discharging cycles, there is a higher probability of noise in timing, causing an arrival at the switching threshold faster or slower. Though, the intensity of this trend is apparently affected by loads. In version 1 under a 100 Ω load, jitter peaked severely, reaching 370.63 µs ($p < 0.05$, $r = 0.701$). Altogether, this shows that operating frequency and timing jitter are strongly correlated.

Jitter varied with circuit modifications too. The most prominent exmaple is in Figure 3.2 where jitters drops from 370.63 µs in version 1 to 183.76 µs in version at a load of 100 Ω. This may be attributed to the addition of decoupling capacitors in version 2 ($p < 0.05$, $r = -0.741$), and it is the only case where power rail RMS noise has a statistically significant

correlation with jitter as can be inferred from Figure 3.3 where, at a 100 Ω, the addition of decoupling in version 2 drastically decreased RMS noise when compared with version 3 or version 1. This suggests that decoupling can improve timing stability in a relaxation oscillator under heavy loads and low operating frequencies (Philips Semiconductors 1988). Besides that, RMS noise does not correlate strongly to changes in jitter.

The comparison between power rail RMS noise and timing jitter in Figure 3.4 further supports this conclusion. The figure shows no clear correlation between power rail RMS noise and timing jitter. Across all versions and loads, RMS noise did not have significant correlation with timing jitter except in the case discussed before. This may be because RMS noise determines the magnitude of noise, not the spectral characteristics necessary to evaluate its effect (Vasilescu 2005).

The results must be explained in the context of the used measurement system. The ESP32 was calibrated and a measurement system based on it was developed for this investigation specifically, as standard laboratory equipment was unavailable. The system was able to measure voltages with ±0.01 V of error after calibration using the ESP-IDF ADC calibration driver (Espressif Systems n.d.), and using continuous ADC allowed the system to fetch input voltage levels at approximately 22.6 kSPS. However, the measurements' resolution was limited by the ADC resolution of the ESP32, and so more accuracy was difficult to establish. On the other side, although the clock frequency was determined through NTP-synchronization to be 80.0006907 MHz, period measurements were quantized as a result of the limitation in clock frequency. Therefore, data should be interpreted in light of these limitations. Even though the measurement system might affect exact numerical values, the overall trends cannot be explained as just error in the measurement system.

Overall, the investigation has shown that factors affecting the performance of relaxation oscillators like the 555 timer's astable mode circuit must be considered separately to characterise its performance more comprehensively. Across the tested versions and environmental conditions, no one version has shown complete superiority to others. Rather, each version had a performace tradeoff, providing an advantage and a disadvantage. Power rail RMS noise was found to weakly correlate with timing jitter relative to other factors like operating frequency and circuit modifications. This shifts the view that jitter is merely a result of power rail disturbances to a view that relaxation oscillators are a dynamic system, where jitter in the output is the result of complex interactions between circuit state variables.

5. Conclusion

This investigation examined the timing behavior of a 555 timer astable oscillator across three circuit configurations, three electrical loads, and eight resistor combinations, with the aim of determining whether power-rail voltage disturbance alone can explain timing jitter. The results indicate that it cannot. While RMS power-rail noise varied only modestly across all tested conditions (approximately 0.02–0.12 V), period jitter varied by more than two orders of magnitude (roughly 3.58 µs to over 360 µs). This disparity indicates that a single scalar noise measurement is insufficient to predict timing stability under the tested conditions.

The three circuit versions each offered distinct advantages rather than a single superior design. Version 1, the unmodified circuit, produced the lowest mean frequency error in lighter loads but suffered from the greatest frequency mean error and variability under the heavy 100 Ω load. Version 2, which added decoupling capacitors, traded some frequency accuracy at higher loads for improved measurement consistency and reduced peak-to-peak voltage transients. Version 3, which added a transistor switching stage, produced the highest mean error at lighter loads but performed best under heavy loading, achieving both the lowest mean frequency error and the greatest suppression of peak-to-peak noise under the 100 Ω condition. No configuration dominated across all metrics, underscoring that circuit modification involves trade-offs among accuracy, stability, and noise suppression rather than a single "best" design.

The jitter results further reinforced the strong influence of operating frequency on timing instability. Jitter decreased sharply as frequency increased, falling below 12 µs at 904.84 Hz across all versions and loads, while reaching its most extreme value of 370.63 µs at 55.98 Hz under heavy loading in Version 1. This pattern is consistent with the relaxation-oscillator mechanism of the 555 timer, and the longer charge/discharge intervals at lower frequencies may allow disturbances in the timing process to produce greater absolute variation in the measured period. Even so, decoupling capacitors measurably reduced jitter under the most demanding low-frequency, heavy-load condition, indicating that supply-noise suppression can still meaningfully improve timing stability in specific operating regimes, even if it is not the dominant factor overall.

These findings were obtained using a custom ESP32-based measurement system developed specifically for this study in the absence of conventional laboratory instrumentation. Careful calibration of both the voltage measurement path (±0.01 V accuracy) and the period measurement path (via MCPWM capture and NTP-based clock calibration, yielding an estimated clock frequency of 80.0006907 MHz) increased

confidence that the observed trends were not dominated by instrumentation error. While residual sources of measurement error, such as ADC reference-voltage variation and nonlinearity, may affect the absolute precision of individual readings, the magnitude of the differences observed between experimental conditions—particularly the two-order-of-magnitude spread in jitter compared to the narrow range of RMS noise—is substantially larger than the measured variation in RMS noise and therefore unlikely to be explained by instrumentation limitations alone.

Taken together, these results reframe the relationship between power-rail disturbance and oscillator timing. Rather than a simple proportional relationship in which reduced voltage noise directly yields reduced jitter, timing stability in the 555 timer emerges from a more complex interaction among operating frequency, electrical loading, and circuit architecture, with RMS noise serving as only a partial and often insufficient predictor. This has practical implications for the design and evaluation of relaxation-oscillator circuits: engineers seeking to optimize a 555 timer–based design should consider the intended operating frequency and loading conditions alongside supply-noise mitigation strategies, rather than treating voltage noise reduction as a proxy for timing performance.

Future work could extend this investigation by incorporating spectral analysis of power-rail disturbances rather than relying solely on RMS and peak-to-peak metrics, since the discussion results suggest that the frequency content of a disturbance, not just its amplitude, may influence its effect on jitter. Additional work could also compare the low-cost ESP32-based instrumentation developed here against calibrated laboratory-grade equipment to further validate its accuracy, and could extend the range of tested frequencies, loads, and circuit modifications to determine whether the trends identified here generalize beyond the tested conditions.

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Biography



Omar Mubarak is a high-school student at the STEM School in El-Minya, Egypt, with interests in coding, electronics, physics, and data analysis. He developed his research skills through ISEF and GPSI, a program offered fully-funded by the Pioneer institute, gaining experience in data analysis, scientific problem-solving, teamwork, and presenting evidence-based solutions.